What Is Claimed Is:

1. A method for manufacturing an electronic product including a field effect transistor, comprising:

providing semiconductor material of a first conductivity type having a surface and two spaced-apart regions along the surface for receiving dopant of a second conductivity type;

forming a field effect transistor gate structure along the surface and over a third region of the surface between the two spaced-apart regions;

providing dopant to the spaced-apart regions;

heating the spaced-apart regions to a temperature at least 50 degrees C higher than the peak temperature which results in the third region when the spaced-apart regions are heated.

2. The method of Claim 1 wherein upon heating the spaced-apart regions the dopant diffuses within the spaced-apart regions and electrically significant amounts of the dopant do not diffuse beyond the spaced-apart regions into other portions of the semiconductor material.

3. The method of claim 1 wherein the peak temperature of the gate structure resulting from heating the spaced-apart regions does not exceed 700C.

4. The method of Claim 1 wherein the step of heating the spaced-apart regions is effected with a monochromatic laser tuned to 308 nm.

5. The method of claim 4 wherein the spaced-apart regions are heated to a temperature at least 300 degrees C higher than the peak temperature which results in the third region when the spaced-apart regions are heated.

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6. An integrated circuit comprising:

a semiconductor material of a first conductivity type having a surface region for formation of devices;

a field effect transistor gate structure formed on the surface region, comprising a conductive layer and an amorphous insulative layer having a dielectric constant greater than five relative to free space, the insulative layer formed between the conductive layer and the surface region;

a source region formed along the surface region and having a second conductivity type; and

a drain region formed along the surface region and having a second conductivity type, said gate structure, source region and drain region configured to form an operable field effect transistor, said source region and said drain region self-aligned with the gate structure.

7. The device of claim 6 wherein the insulative layer comprises Ta_2O_5.

8. The device of claim 6 further including a layer of SiO_2 disposed between the insulative layer and the surface region.

9. A semiconductor device comprising:

a semiconductor material of a first conductivity type having a surface region for formation of devices;

a field effect transistor gate structure formed on the surface region, comprising a conductive layer and an insulative layer having a dielectric constant greater than 5 relative to free space, the insulative layer formed between the conductive layer and the surface region; and

a source region and a drain region each formed in the surface region, aligned with the gate structure and on a different side of the gate structure,

said gate structure, source region and drain region configured to form a field effect transistor characterized by a gate leakage current less than 0.1 amp per cm^{-2} during operation.

10. The device of claim 9 wherein the field effect transistor is characterized by a gate leakage current less than 10 milliamps per cm^{-2} during operation.

11. The device of claim 9 wherein the field effect transistor is characterized by a gate leakage current less than one milliamp per cm^{-2} during operation.

12. A method for manufacturing a semiconductor electronic product comprising:

providing semiconductor material having a surface region;

providing dopant to a portion of the surface region;

irradiating the portion of the surface region with sufficient energy to induce diffusion of the dopant from the portion of the surface region to another region of the semiconductor material.

13. The method of claim 12 wherein the step of irradiating elevates the temperature of the portion of the surface region to render the dopant soluble in the semiconductor material.

14. The method of claim 12 wherein the step of irradiating renders the portion of the surface region liquid.

15. The method of claim 13 wherein the step of irradiating renders a portion of the semiconductor material including said portion of the surface region liquid and results in diffusion of the dopant about the liquid portion without electrically significant amounts of the dopant diffusing out of the liquid portion to other portions of the semiconductor material.

16. The method of claim 12 including the step of allowing the liquid region to solidify.

17. A method for controlling movement of a dopant species in a semiconductor material comprising:

providing semiconductor material having a plurality of adjoining regions with a surface for formation of electronic devices;

introducing the dopant species along the surface of a first of the regions of the semiconductor material;

elevating the temperature of the first region of the semiconductor material relative to the temperature of a surrounding region of the semiconductor material such that the dopant diffuses within at least a portion of the first region.

18. The method of claim 17 wherein upon elevation of the temperature in the first region the temperature of the surrounding region remains lower than the minimum temperature required to effect thermal diffusion of the dopant species in the surrounding region.

19. The method of claim 17 wherein elevation of the temperature in the first region is of such limited time duration as to preclude diffusion of electrically significant amounts of the dopant species into the surrounding region.

20. A method for manufacturing a semiconductor electronic product comprising:

providing semiconductor material having a surface region with a layer of SiO_2 formed thereon and a layer comprising a metal also formed thereon;

providing dopant to a portion of the surface region;

irradiating the surface region so that the portion of the surface region containing the dopant absorbs sufficient radiation to diffuse the dopant into another portion of the semiconductor material while at least one of the layers formed on the surface region reflects radiation.

21. The method of claim 18 wherein the layer of metal comprises tungsten silicide.

22. A method for manufacturing an electronic product including a field effect transistor, comprising:

providing semiconductor material of a first conductivity type having a surface and two spaced-apart regions along the surface for receiving dopant of a second conductivity type;

forming a field effect transistor gate structure along the surface and over a third region of the surface between the two spaced-apart regions;

providing dopant to the spaced-apart regions;

heating the spaced-apart regions with laser radiation.

23. A method for manufacturing an electronic product including a field effect transistor, comprising:

providing semiconductor material of a first conductivity type having a surface and two spaced-apart regions along the surface for receiving dopant of a second conductivity type;

forming a field effect transistor gate structure along the surface and over a third region of the surface between the two spaced-apart regions;

providing dopant to the spaced-apart regions;

heating the spaced-apart regions by applying radiation of a wavelength which is capable of being absorbed by the spaced-apart regions and reflected by a portion of the gate structure.